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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,496	01/10/2002	Binyu Zang	42390P13145	9184

8791	7590	11/19/2004

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EXAMINER
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ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/043,496	ZANG ET AL.
	Examiner	Art Unit	
	Chih-Ching Chow	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _10 January 2002_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-30_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-30_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _10 January 2002_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _04/15/2002_.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on January 10, 2002.

2. The priority date considered for this application is January 10, 2002.

3. Claims 1-30 have been examined.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 11, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. As per independent claims 1, 11, and 21 recites: "a first last use of a first canonical register in a block of code", where 'first last use of a first canonical register' is not clearly defined as to what are included and what are excluded. Examiner assumes that this paragraph means 'the last value of a canonical register'. Further more, claims 1, 11, and 21 recites: "a first rollback and a first recovery to the first original register based on whether the recorded first last use occurs before a first last definition of the first original register in the block of code.", where 'first rollback and a first recovery....first last use occurs before a first last

definition..." -- Is the first rollback or first recovery only for the first original register, and second rollback or second recovery only for the second original register? What is the difference between a first last <u>use</u> and a first last <u>definition</u>? And how to determine 'recorded first last use occurs <u>before</u> a first last definition of the first original register'? It's not clear if the 'recording' is done for the contents of the register or also for the time when the register is modified; again, it is not clearly defined as to what are included and what are excluded. Thus, claims 2-10, 12-20, and 22-30 are also rejected on, for being dependent on rejected base claims, respectively. Appropriate corrections are required.

Examiner assumes that the claim means 'do rollback or recovery for the first original register if its current value is different from the first canonical register based on the time which was recorded in the canonical register'; the 'original registers' are 'logical registers', the 'canonical registers' are physical registers; and the temporary registers are implemented as a mapping table which maps the logical registers to the physical registers; it can keep track of which temporary register has been stored in each of the physical registers and when the related instruction is done, it removes the content from table (rollback) and install the

previously stored value into the original register (recovery) – this process repeats

for the first original register to the last original register.

7.   Claims 3-5, 13-15, and 23-25 are rejected under 35 U.S.C. 112, second

paragraph, as being indefinite for failing to particularly point out and distinctly

claim the subject matter which applicant regards as the invention.

8.   As per independent claims 3-5, 13-15, and 23-25 recites: "a first target

register", which is not clearly defined as to what are included and what are

excluded. Examiner assumes that 'a first target register' means the first

temporary register, which the canonical register is mapped to.

9.   Claims 5, 15, and 25 are rejected under 35 U.S.C. 112, second paragraph, as

being indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention.

10.   As per independent claims 6-8, 16-18, and 26-28 recites: "second last use of

a second canonical register", a "second last definition of the second original

register", and a "second last write to the second target register", where the

'second last use', the 'second last definition', and the 'second last write' are not

clearly defined as to what are included and what are excluded. Examiner assumes

that means the second available value in the temporary register, which the

canonical register is mapped to.

Claim Rejections - 35 USC § 103

11.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as
> set forth in section 102 of this title, if the differences between the subject matter sought to
> be patented and the prior art are such that the subject matter as a whole would have been
> obvious at the time the invention was made to a person having ordinary skill in the art to which
> said subject matter pertains. Patentability shall not be negatived by the manner in which the
> invention was made.

12.   Claims 1, 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable

over U.S. Patent No. 5,758,112 by Kenneth C. Yeager (hereinafter "Yeager"), in

view of US 2004/0186981 by David S. Christie (hereinafter "Christie") .

CLAIM

1. A method comprising:

   (a) recording a first last use of a first canonical register in a block of code after a renaming, the first canonical register being mapped to a first original register; and

   (b) applying one of a first rollback and a first recovery to the first original register based on whether the recorded first last use occurs before a first last definition of the first original register in the block of code.

Yeager / Christie

For item (a), in Yeager, column 6, lines 25-34, "**Register renaming** is a technique used to keep track of changing register values. Processor 100 generates a myriad of temporary register results as it executes instructions. These temporary values, along with permanent values, are **stored** (*recording*) in register files 302 or 306 along with permanent values. Temporary values become new permanent values when the corresponding instructions graduate. Renaming identifies where the current (temporary or permanent) value of each register is in the register file."

For item (b), in Yeager, column 7, lines 33-35, "mapping table 206 reflects the **latest** (*last definition*) mapping of logical destination register number 256. The **old** physical destination 282 associated with logical number 256 is output (*rollback*) from mapping table 206 and appended to active list (*recovery*)".

Yeager teaches all aspects of claim 1 but does not mention the 'block of code' specifically. However, Christie teaches these features in an analogous art. In in Christie, paragraph 45, "in this particular implementation, MMU 20 generates the operating mode responsive to a **code segment** descriptor corresponding to the **code being**

executed (*block of code*) and further responsive to one or more values in control registers." And paragraph 78, " such a processor embodiment may execute interpreter software which reads each non-native instruction in a non-native code sequence as data, and executes **various software routines** (*block of code*) which emulate the defined operation of the non-native instruction as defined in the non-native processor architecture." In paragraph 40, "Alternatively, execution core 14 may employ a form of **register renaming** in which **any register within register file 22 may be mapped to an architected register.**" Also, in paragraph, 0105, "FIG. 10 illustrates **mapping the general registers 1052 to registers in register file 1044,** any other non-native architected state may be mapped to registers in register file 1044. For example, **any of segment registers 1054, control registers 1056, or other registers** 1058 (or portions of any of these registers) may be mapped to register file 1044, as desired." Christie teaches the 'renaming of the register', but he is using the 'mapping' instead of the 'renaming'. Christie's 'general register', 'control register' or 'other register' basically function the same as the 'original register', 'temporary register' and the 'canonical register' as recited in current application.

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Yeager's disclosure of the register renaming with utilizing it for 'block of code' concept taught by Christie, for the purpose of corresponding the code being executed to one or more values in control registers. (see Christie, paragraph 45, 1st sentence).

2. The method of claim 1 wherein applying one of the first rollback and the first recovery comprises:

(a) applying the first rollback to the first original register if the recorded first last use occurs before the first last definition of the first original register; and

(b) applying the first recovery to the first original register if the recorded first last use does not occur before the first last definition of the first original register.

For the feature of claim 1 see claim 1 rejection. In Yeager, Column 14, lines 33-35, "When an instruction graduates, the "old" (*determining the 'before' situation in item (b)*) physical register number associated with its destination register is written back (*rollback*) into the appropriate free list."

3. The method of claim 2 wherein applying the first rollback comprises:

(a) replacing a first reference to a first target register with the first canonical register when the first reference is a destination of a first last write to the first target register, the first target register corresponding to the first original register after the renaming; and

For the feature of claim 2 see claim 2 rejection. For the rest of the feature in claim 3 see claim 1 rejection.

(b) replacing a second reference to the first target register with the first canonical register when the second reference is a source of a first operation after the first last write to the first target register.

4. The method of claim 2 wherein applying the first recovery comprises:
  copying the first target register to the first canonical register at end of the block.

For the feature of claim 2 see claim 2 rejection. See claim 1 rejection, where "temporary values become new permanent values" means the **copying** the target register to the first canonical register.

5. The method of claim 4 wherein copying the first target register comprises:
  (a) copying the first target register to a first unused temporary register; and
  (b) copying the first unused temporary register to the first canonical register.

For the feature of claim 4 see claim 4 rejection, for the rest of the feature of claim 5 see claim 4 rejection.

6. The method of claim 5 further comprises:
  (a) recording a second last use of a second canonical register in the block of code after the renaming, the second canonical register being mapped to a second original register; and
  (b) applying one of a second rollback and a second recovery to the second original register based on whether the recorded second last use of the second canonical register occurs before a second last definition of the second original register in the block of code.

For the feature of claim 5 see claim 5 rejection. For the rest of the features see claim 1 rejection.

7. The method of claim 6 wherein applying one of the second rollback and the second recovery comprises:

(a) applying the second rollback to the second original register if the recorded second last use occurs before the second last definition of the second original register; and

(b) applying the second recovery to the second original register if the recorded second last use does not occur before the second last definition of the second original register.

For the feature of claim 6 see claim 6 rejection. For the rest of the features see claim 2 rejection.

8. The method of claim 7 wherein applying the second rollback comprises:

(a) replacing a third reference to a second target register with the second canonical register when the third reference is a destination of a second last write to the second target register, the second target register corresponding to the second original register after the renaming; and

(b) replacing a fourth reference to the second target register with the second canonical register when the fourth reference is a source of a second operation after the second last write to the second target register.

For the feature of claim 7 see claim 7 rejection. For the rest of the features see claim 3 rejection.

9. The method of claim 8 wherein applying the second recovery comprises:

(a) copying the second target register to the second canonical register at end

For the feature of claim 8 see claim 8 rejection. For the rest of the features see claim 4 rejection.

of the block.

10. The method of claim 9 wherein copying the second target register comprises:

  (a) copying the second target register to a second unused temporary register before copying the first unused temporary register to the first canonical register; and

  (b) copying the second unused temporary register to the second canonical register.

For the feature of claim 9 see claim 9 rejection. For rest of the features see claim 5 rejection.

11. A computer program product comprising:

  (a) a machine useable medium having program code embedded therein, the program code comprising:

  (i) computer readable program code to record a first last use of a first canonical register in a block of code after a renaming, the first canonical register being mapped to a first original register; and

  (ii) computer readable program code to apply one of a first rollback and a first recovery to the first original register based on whether the recorded first last use occurs before a first last definition of the first original register in the block of code.

Both Yeager's FIG. 1 (Instruction Cache) and Christie's Fig. 13 (L2 Cache) teaches a machine useable medium having code embedded therein. For the rest of feature 11, same as claim 1 rejection.

12. The computer program product of claim 11 wherein the computer readable program code to apply one of the first

For the feature of claim 11 see claim 11 rejection. For rest of the features see claim 2 rejection.

rollback and the first recovery comprises:

(a) computer readable program code to apply the first rollback to the first original register if the recorded first last use occurs before the first last definition of the first original register; and

(b) computer readable program code to apply the first recovery to the first original register if the recorded first last use does not occur before the first last definition of the first original register.

13. The computer program product of claim 12 wherein the computer readable program code to apply the first rollback comprises:

(a) computer readable program code to replace a first reference to a first target register with the first canonical register when the first reference is a destination of a first last write to the first target register, the first target register corresponding to the first original register after the renaming; and

(b) computer readable program code to replace a second reference to the first target register with the first canonical register when the second reference is a source of a first operation after the first last write to the first target register.

For the feature of claim 12 see claim 12 rejection. For rest of the features see claim 3 rejection.

14. The computer program product of

For the feature of claim 12 see claim 12

claim 12 wherein the computer readable program code to apply the first recovery comprises:

computer readable program code to copy the first target register to the first canonical register at end of the block.

rejection. For rest of the features see claim 4 rejection.

15. The computer program product of claim 14 wherein the computer readable program code to copy the first target register comprises:

(a) computer readable program code to copy the first target register to a first unused temporary register; and

(b) computer readable program code to copy the first unused temporary register to the first canonical register.

For the feature of claim 14 see claim 14 rejection. For rest of the features see claim 5 rejection.

16. The computer program product of claim 15 further comprises:

(a) computer readable program code to record a second last use of a second canonical register in the block of code after the renaming, the second canonical register being mapped to a second original register; and

(b) computer readable program code to apply one of a second rollback and a second recovery to the second original register based on whether the recorded second last use of the second canonical register occurs before a second last definition of the second original register in the block of code.

For the feature of claim 15 see claim 15 rejection. For rest of the features see claim 6 rejection.

17. The computer program product of claim 16 wherein the computer readable program code to apply one of the second rollback and the second recovery comprises:

  (a) computer readable program code to apply the second rollback to the second original register if the recorded second last use occurs before the second last definition of the second original register; and

  (b) computer readable program code to apply the second recovery to the second original register if the recorded second last use does not occur before the second last definition of the second original register.

For the feature of claim 16 see claim 16 rejection. For rest of the features see claim 7 rejection.

18. The computer program product of claim 17 wherein the computer readable program code to apply the second rollback comprises:

  (a) computer readable program code to replace a third reference to a second target register with the second canonical register when the third reference is a destination of a second last write to the second target register, the second target register corresponding to the second original register after the renaming; and

  (b) computer readable program code to replace a fourth reference to the second target register with the second canonical register when the fourth reference is a source of a second

For the feature of claim 17 see claim 17 rejection. For rest of the features see claim 8 rejection.

operation after the second last write to the second target register.

19. The computer program product of claim 18 wherein the computer readable program code to apply the second recovery comprises: computer readable program code to copy the second target register to the second canonical register at end of the block.	For the feature of claim 18 see claim 18 rejection. For rest of the features see claim 9 rejection.
20. The computer program product of claim 19 wherein the computer readable program code to copy the second target register comprises: (a) computer readable program code to copy the second target register to a second unused temporary register before copying the first unused temporary register to the first canonical register; and (b) computer readable program code to copy the second unused temporary register to the second canonical register.	For the feature of claim 19 see claim 19 rejection. For rest of the features see claim 10 rejection.
21. A system comprising: (a) a processor; and (b) a memory coupled to the processor to store program code, the program code, when executed, causing the processor to: (i) record a first last use of a first canonical register in a block of code after a renaming, the first canonical	Both Yeager's FIG. 1 (Superscalar Processor Architecture) and Christie's Fig. 13 (Processor) teaches a system with a processor and memory to store program code. For the rest of feature 21, same as claim 1 rejection.

register being mapped to a first original
register; and

(ii) apply one of a first rollback and a
first recovery to the first original
register based on whether the recorded
first last use occurs before a first last
definition of the first original register
in the block of code.

22. The system of claim 21 wherein the
program code causing the processor to
apply one of the first rollback and the
first recovery causes the processor to:

(a) apply the first rollback to the first
original register if the recorded first
last use occurs before the first last
definition of the first original register;
and

(b) apply the first recovery to the
first original register if the recorded
first last use does not occur before the
first last definition of the first original
register.

For the feature of claim 21 see claim 21
rejection. For rest of the features see
claim 2 rejection.

23. The system of claim 22 wherein the
program code causing the processor to
apply the first rollback causes the
processor to:

(a) replace a first reference to a first
target register with the first canonical
register when the first reference is a
destination of a first last write to the
first target register, the first target
register corresponding to the first
original register after the renaming; and

(b) replace a second reference to the

For the feature of claim 22 see claim 22
rejection. For rest of the features see
claim 3 rejection.

first target register with the first
canonical register when the second
reference is a source of a first
operation after the first last write to
the first target register.

24. The system of claim 22 wherein the
program code causing the processor to
apply the first recovery causes the
processor to:
 (a) copy the first target register to
the first canonical register at end of
the block.

For the feature of claim 22 see claim 22
rejection. For rest of the features see
claim 4 rejection.

25. The system of claim 24 wherein the
program code causing the processor to
copy the first target register causes
the processor to:
 (a) copy the first target register to a
first unused temporary register; and
 (b) copy the first unused temporary
register to the first canonical register.

For the feature of claim 24 see claim 24
rejection. For rest of the features see
claim 5 rejection.

26. The system of claim 25 wherein the
program code further causes the
Processor to:
 (a) record a second last use of a
second canonical register in the block of
code after the renaming, the second
canonical register being mapped to a
second original register; and
 (b) apply one of a second rollback and a
second recovery to the second original
register based on whether the recorded
second last use of the second canonical
register occurs before a second last

For the feature of claim 25 see claim 25
rejection. For rest of the features see
claim 6 rejection.

definition of the second original
register in the block of code.

27. The system of claim 26 wherein the
program code causing the processor to
apply one of the second rollback and the
second recovery causes the processor
to:

(a) apply the second rollback to the
second original register if the recorded
second last use occurs before the
second last definition of the second
original register; and

(b) apply the second recovery to the
second original register if the recorded
second last use does not occur before
the second last definition of the second
original register.

For the feature of claim 26 see claim 26
rejection. For rest of the features see
claim 7 rejection.

28. The system of claim 27 wherein the
program code causing the processor to
apply the second rollback causes the
processor to:

(a) replace a third reference to a
second target register with the second
canonical register when the third
reference is a destination of a second
last write to the second target register,
the second target register
corresponding to the second original
register after the renaming; and

(b) replace a fourth reference to the
second target register with the second
canonical register when the fourth
reference is a source of a second
operation after the second last write to

For the feature of claim 27 see claim 27
rejection. For rest of the features see
claim 8 rejection.

the second target register.

29. The system of claim 28 wherein the program code causing the processor to apply the second recovery causes the processor to: (a) copy the second target register to the second canonical register at end of the block.	For the feature of claim 28 see claim 28 rejection. For rest of the features see claim 8 rejection.

30. The system of claim 29 wherein the program code causing the processor to copy the second target register causes the processor to:
 	
  (a) copy the second target register to a second unused temporary register before copying the first unused temporary register to the first canonical register; and
 	
  (b) copy the second unused temporary register to the second canonical register.
	For the feature of claim 29 see claim 20 rejection. For rest of the features see claim 10 rejection.

Conclusion

13.   The following summarizes the status o f the claims:

   35 USC § 112 (2nd) claim rejection: claims 1-30

   35 USC § 103 claim rejection: claims 1-30

14.   The prior arts made of record and not relied upon is considered pertinent to applicant's disclosure:

   Le, Bich-Cau, U.S. Patent No. 6,631,514 discloses a method for defining the dynamic legacy-to-native register mappings.

Rechtschaffen, Rudolph Nathan et al., **U.S. Patent No. 5,802,338** discloses an method and apparatus, which when an instruction causes a register to be modified, the register is renamed to the sequentially next higher register that has not as yet been used. The new name of the register is placed in a register correspondence table and any reference to the architected register name will have that name translated to its rename value.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Ching Chow whose telephone number is 571-272-3693. The examiner can normally be reached on 7:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chih-Ching Chow
Examiner
Art Unit 2122

CC

ANTONY NGUYEN-BA
PRIMARY EXAMINER